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EXAMINER	
KIM, HONG CHONG	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 12/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/828,283	MOBLEY, KENNETH J.	
	Examin r	Art Unit	
	Hong C Kim	2186	

-- The MAILING DATE of this communication appears on the c ver sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3,5-7,10-13,16,17,20 and 25-31* is/are allowed.

6)☒ Claim(s) *4,8,9,14,15,18,19 and 21-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

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Detailed Action

1. Claims 1-31 are presented for examination. This office action is in response to the RCE filed on 10/18/2004.

2. The examiner requests, in response to this Office action, any reference(s) known to qualify as prior art under 35 U.S.C. sections 102 or 103 with respect to the invention as defined by the independent and dependent claims. That is, any prior art (including any products for sale) similar to the claimed invention that could reasonably be used in a 102 or 103 rejection. This request does not require applicant to perform a search. This **request** is not intended to interfere with or go beyond that **required** under 37 C.F.R. 1.56 or 1.105.

The request may be fulfilled by asking the attorney(s) of record handling prosecution and the inventor(s)/assignee for references qualifying as prior art. A simple statement that the query has been made and no prior art found is sufficient to fulfill the request. Otherwise, the fee and certification requirements of 37 CFR section 1.97 are waived for those documents submitted in reply to this request. This waiver extends only to those documents within the scope of this request that are included in the application's first complete communication responding to this requirement. Any supplemental replies subsequent to the first communication responding to this request and any information disclosures beyond the scope of this are subject to the fee and certification requirements of 37 CFR section 1.97.

In the event prior art documentation is submitted, a discussion of relevant

passages, figs. etc. with respect to the claims is requested. The examiner is looking for specific references to 102/103 prior art that identify independent and dependent claim limitations. Since applicant is most knowledgeable of the present invention and submitted art, his/her discussion of the reference(s) with respect to the instant claims is essential. **A response to this inquiry is greatly appreciated.**

The examiner also requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line number(s), in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

Claim Objections

3. Claims 14 and 18 are objected to because of the following informalities: In step (c) "on e" should be changed to –one--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. Claims 8-9, 18-19, 21-24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As to claims 8-9, 18-19 and 21-24, it appear that "'the refresh circuitry further comprises a refresh timer for setting a minimum time between refresh cycles" was not described in the specification at the time the application was filed. It appears that applicant also sets to maximum value (see page 5 lines 4-20 "time has expired" and "reset to its maximum value". In other words, a refresh timer set to the maximum allowable value since it may adversely waste power by running refreshes excessively).

As to claims 21-24, it appear that "a comparator for internally determining when a refresh cycle can be hidden behind an access to the non-array row" was not described in the specification at the time the application was filed. It appears that "comparator" (two occurrences) should be changed to –a command decoder--.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 21 are rejected under 35 USC § 103(a) as being unpatentable over *Alwais et al, (Alwais)* U.S. Patent 5,991,851 in view of Novak et al. (Novak) U.S. Patent 6,147,921.

As to claim 21, Alwais discloses the invention as claimed. Alwais discloses a memory device (Fig. 1) having a non-array row external (Fig. 1 Ref. 14) to plural DRAM sub-arrays (Fig. 1 Refs. 12s), for receiving from the DRAM sub-array referenced by an address of an access request comprising: a command decoder (Fig. 1 Ref. 18 and col. 9 lines 1-3) for internally determining when a refresh cycle can be hidden behind an access to the non-array row; and a controller (Fig. 1 Ref. 28) for limiting refresh cycles to a subset of possible times internally determined by the command decoder, however, Alwais does not specifically disclose setting a minimum time between refresh cycles based on a refresh timer.

Novak discloses setting a minimum time between refresh cycles based on a refresh timer (col. 7 lines 38-51) for the purpose of providing optimum refresh time thereby data retention is guaranteed.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate setting a minimum time between refresh cycles based on a refresh timer as taught by Novak into the system of Alwais for the advantages stated above.

6. Claim 22 is rejected under 35 USC § 103(a) as being unpatentable over *Alwais et al, (Alwais)* U.S. Patent 5,991,851 in view of Novak et al. (Novak) U.S. Patent 6,147,921 and further in view of Dosaka et al. (Dosaka) U.S. Patent 5,559,750 or applicant admitted prior art (AAPA).

As to claim 22, Alwais and Novak disclose the invention as claimed above.

However, neither Alwais nor Novak specifically discloses wherein the non-array row comprises an SRAM row.

Dosaka discloses wherein the non-array row comprises at an SRAM row is disclosed by Dosaka (Fig. 1 Ref. 506) or AAPA (page 2 line 7) for the purpose of decreasing foot print, size, and/or power.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate wherein the non-array row comprises an SRAM row as taught by Dosaka or AAPA into the combined invention of Alwais and Novak for the advantages stated above.

7. Claim 23 is rejected under 35 USC § 103(a) as being unpatentable over *Alwais et al, (Alwais)* U.S. Patent 5,991,851 in view of Novak et al. (Novak) U.S. Patent 6,147,921 and further in view of Ghosh et al. (Ghosh) U.S. Patent 5,619,468 .

As to claim 23, Alwais and Novak disclose the invention as claimed above. However, neither Alwais nor Novak specifically discloses wherein the controller comprises a missed refresh counter for tracking a number of refreshes missed by at least one of the plural DRAM sub-arrays.

Ghosh discloses wherein the controller comprises a missed refresh counter for tracking a number of refreshes missed by at least one of the plural DRAM sub-arrays (col. 4 lines 55-56) for the purpose of providing proper refresh timing thereby data retention is guaranteed.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate wherein the controller comprises a refresh timer for setting a minimum time between refresh cycles as taught by Gosh into the combined invention of Alwais and Novak for the advantages stated above.

8. Claim 24 is rejected under 35 USC § 103(a) as being unpatentable over *Alwais et al, (Alwais)* U.S. Patent 5,991,851 in view of Novak et al. (Novak) U.S. Patent 6,147,921 and further in view of Takemae et al. (Takemae) U.S. Patent 5,619,468 .

As to claim 24, Alwais and Novak disclose the invention as claimed above. However, neither Alwais nor Novak specifically discloses the controller further comprises a refresh counter for storing a next array row to be refreshed in at least one of the plural DRAM sub-arrays.

Takemae discloses the controller further comprises a refresh counter for storing a next array row to be refreshed in at least one of the plural DRAM sub-arrays (col. 8 lines 6-10) for the purpose of providing proper address range thereby data retention is guaranteed.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the controller further comprises a refresh counter for storing a next array row to be refreshed in at least one of the plural DRAM sub-arrays as taught by Takemae into the combined invention of Alwais and Novak for the advantages stated above.

9. Claim 4 is rejected under 35 USC § 103(a) as being unpatentable over *Alwais et al, (Alwais)* U.S. Patent 5,991,851 in view of Dosaka et al. (Dosaka) U.S. Patent 5,559,750 or applicant admitted prior art (AAPA).

As to claim 4, *Alwais*, discloses a memory device having plural DRAM sub-arrays (fig. 3 Refs 12s), each with plural array rows comprising: an address decoder (Fig. 1 Ref. 18) for decoding an address of a memory access request and indicating which of the plural DRAM sub-arrays are referenced by the memory access request; and refresh circuitry (Fig. 1 Ref. 28), responsive to the indication of the address decoder, to refresh at least one array row of at least one of the plural DRAM sub-arrays not referenced by the memory access request while contemporaneously performing the memory request (col. 4 lines 40-61, col. 9 lines 5-12, 22-25, and col. 12 lines 22-24) , a non-array row (Fig. 1 Ref. 14) external to the DRAM sub-arrays for receiving from the DRAM sub-array referenced by the address of the memory access request at least a portion of an array row corresponding to the address of the memory access request (col. 4 lines 40-61 and col. 6 lines 6-33).

However, Alwais does not specifically disclose wherein the non-array row comprises at most one SRAM row.

Dosaka discloses wherein the non-array row comprises at most one SRAM row is disclosed by Dosaka (Fig. 1 Ref. 506) or AAPA (page 2 line 7) for the purpose of decreasing foot print, size, and/or power.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate wherein the non-array row comprises at

most one SRAM row as taught by Dosaka or AAPA into the system of Alwais for the advantages stated above.

10. Claim 8 is rejected under 35 USC § 103(a) as being unpatentable over *Alwais et al, (Alwais)* U.S. Patent 5,991,851 in view of Novak et al. (Novak) U.S. Patent 6,147,921.

As to claim 8, *Alwais*, discloses a memory device having plural DRAM sub-arrays (fig. 3 Refs 12s), each with plural array rows comprising: an address decoder (Fig. 1 Ref. 18) for decoding an address of a memory access request and indicating which of the plural DRAM sub-arrays are referenced by the memory access request; and refresh circuitry (Fig. 1 Ref. 28), responsive to the indication of the address decoder, to refresh at least one array row of at least one of the plural DRAM sub-arrays not referenced by the memory access request while contemporaneously performing the memory request (col. 9 lines 5-12, 22-25, and col. 12 lines 22-24), a non-array row (Fig. 1 Ref. 14) external to the DRAM sub-arrays for receiving from the DRAM sub-array referenced by the address of the memory access request at least a portion of an array row corresponding to the address of the memory access request (col. 6 lines 6-33 and col. 4 lines 40-61).

However, Alwais does not specifically disclose wherein the refresh circuitry further comprises a refresh timer for setting a minimum time between refresh cycles.

Novak discloses wherein the refresh circuitry further comprises a refresh timer for setting a minimum time between refresh cycles (col. 7 lines 38-51) for the purpose of providing optimum refresh time thereby data retention is guaranteed.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate wherein the refresh circuitry further comprises a refresh timer for setting a minimum time between refresh cycles as taught by Novak into the system of Alwais for the advantages stated above.

11. Claim 9 is rejected under 35 USC § 103(a) as being unpatentable over *Alwais et al, (Alwais)* U.S. Patent 5,991,851 in view of Novak et al. (Novak) U.S. Patent 6,147,921 and further in view of Ghosh et al. (Ghosh) U.S. Patent 5,619,468 .

As to claim 9, Alwais and Novak disclose the invention as claimed above. However, neither Alwais nor Novak specifically discloses wherein the refresh circuitry further comprises a missed refresh counter for tracking a number of refreshes missed by at least one of the plural DRAM sub-arrays.

Ghosh discloses wherein the refresh circuitry further comprises a missed refresh counter for tracking a number of refreshes missed by at least one of the plural DRAM sub-arrays (col. 4 lines 55-56) for the purpose of providing proper refresh timing thereby data retention is guaranteed.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate wherein the refresh circuitry further comprises a refresh timer for setting a minimum time between refresh cycles as taught

by Ghosh into the combined invention of Alwais and Novak for the advantages stated above.

12. Claims 14-15 are rejected under 35 USC § 103(a) as being unpatentable over *Alwais et al, (Alwais)* U.S. Patent 5,991,851 in view of Dosaka et al. (Dosaka) U.S. Patent 5,559,750 or applicant admitted prior art (AAPA).

As to claim 14, *Alwais*, discloses a method of refreshing a memory device having a plural DRAM sub-arrays (fig. 3 Refs 12s), each with plural array rows the method comprising: decoding (Fig. 1 Ref. 18) address of a memory access request; indicating (Fig. 1 Ref. 18) which of the plural DRAM sub-arrays are referenced by the memory access request; and refreshing (Fig. 1 Ref. 28), in responsive to the indicating step, at least one array row of at least one of the plural DRAM sub-arrays not referenced by the memory access request (col. 9 lines 5-12, 22-25, and col. 12 lines 22-24), executing the memory address request (col. 6 lines 4-6), and receiving, into a non-array row (Fig. 1 Ref. 14) external to the DRAM sub-arrays for receiving from the DRAM sub-array referenced by the address of the memory access request at least a portion of an array row corresponding to the address of the memory access request (col. 4 lines 40-61 and col. 6 lines 6-33), wherein third stop and fourth steps are performed contemporaneously (col. 9 lines 5-12, 22-25, and col. 12 lines 22-24).

However, Alwais does not specifically disclose wherein the non-array row comprises at most one SRAM row.

Dosaka discloses wherein the non-array row comprises at most one SRAM row is disclosed by Dosaka (Fig. 1 Ref. 506) or AAPA (page 2 line 7) for the purpose of decreasing foot print, size, and/or power.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate wherein the non-array row comprises at most one SRAM row as taught by Dosaka or AAPA into the system of Alwais for the advantages stated above.

As to claim 15, Alwais, Dosaka and AAPA disclose the invention as claimed above. Alwais further discloses storing in a tag register (col. 4 line 41, cache reads on this limitation since a cache stores an address (tag) and data in cache memory) at least a portion of the address of a read access request that last stored information into the non-array row; and comparing (col. 4 lines 47-61) whether the read access request may be serviced from the non-array row rather than the array row corresponding to the address of the read access request.

13. Claims 18-19 are rejected under 35 USC § 103(a) as being unpatentable over *Alwais et al, (Alwais)* U.S. Patent 5,991,851 in view of Novak et al. (Novak) U.S. Patent 6,147,921.

As to claim 18, *Alwais*, discloses a method of refreshing a memory device having a plural DRAM sub-arrays (fig. 3 Refs 12s), each with plural array rows the method comprising: decoding (Fig. 1 Ref. 18) address of a memory access request; indicating

(Fig. 1 Ref. 18) which of the plural DRAM sub-arrays are referenced by the memory access request; and refreshing (Fig. 1 Ref. 28), in responsive to the indicating step, at least one array row of at least one of the plural DRAM sub-arrays not referenced by the memory access request (col. 9 lines 5-12, 22-25, and col. 12 lines 22-24), and executing the memory address request (col. 6 lines 4-6), wherein third stop and fourth steps are performed contemporaneously (col. 9 lines 5-12, 22-25, and col. 12 lines 22-24).

However, Alwais does not specifically disclose setting a minimum time between refresh cycles based on a refresh timer.

Novak discloses setting a minimum time between refresh cycles based on a refresh timer (col. 7 lines 38-51) for the purpose of providing optimum refresh time thereby data retention is guaranteed.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate setting a minimum time between refresh cycles based on a refresh timer as taught by Novak into the system of Alwais for the advantages stated above.

As to claim 19, Alwais and Novak disclose the invention as claimed above. Novak further discloses tracking a number of refreshes missed by at least one of the plural DRAM sub-arrays (col. 7 lines 38-51).

Allowable Subject Matter

14. Claim 1-3, 5-7, 10, 25, 26, 11-13, 16, 17, 20, and 27-31 are allowed.

Response to Arguments

15. Applicant's arguments with respect to claims 1-31 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

2. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

3. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

4. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references

cited to assist examiner to locate the appropriate paragraphs.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong C Kim whose telephone number is 703-272-4181. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached on (703) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to TC-2100:
(703) 872-9306

HK
Primary Patent Examiner
December 11, 2004